IDEC Chip Design Contest

28-nm CMOS Chipset for Optical Interconnects

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Introduction

- The demand for faster, cost-effective, and energy-efficient interconnect solutions is increasing for deep learning and cloud computing applications in data centers
- Optical interconnects offer higher bandwidth, reduced electromagnetic interference, and improved long-distance data efficiency compared to electrical interconnects.
- This work presents the 40-Gb/s VCSEL driver reconfigurable 3-tap fractionally spaced FFE and the inductor-less 28-Gb/s optical receiver analog front-end optimization using Berkeley analog generator in the 28-nm process.

VCSEL Driver

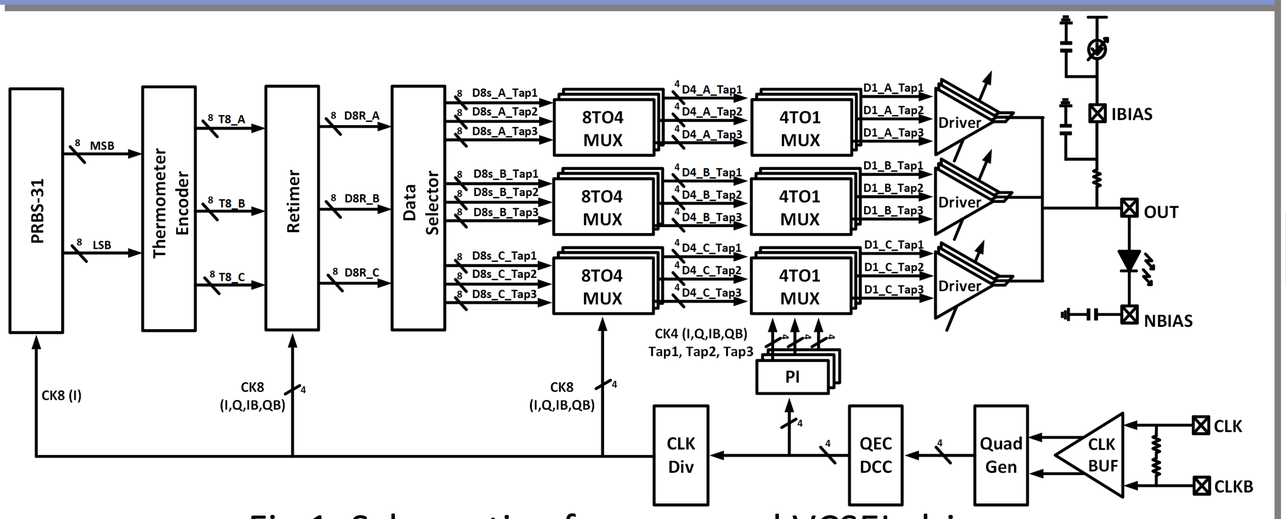
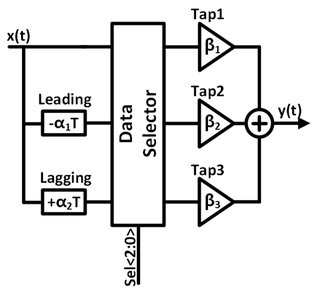


Fig 1. Schematic of a proposed VCSEL driver.

- The proposed VCSEL driver consists of PRBS-31, thermometer encoder, re-timer, data selector for reconfigurable FFE, 16:1 serializer, phase interpolator for fractionally spaced FFE, output buffer, and VCSEL.



Sel <2:0>	Tap1	Tap2	Tap3	Cursor (Tap1, Tap2, Tap3)
000	x(t)	x(t)	x(t)	main, main, main
001	x(t)	x(t+α_1T)	0	main, pre, off
010	x(t)	x(t-α_2T)	0	main, post, off
011	x(t)	x(t)	x(t+α_1T)	main, main, pre
100	x(t)	x(t)	x(t-α_2T)	main, main, post
101	x(t)	x(t+α_1T)	x(t-α_2T)	main, pre, post

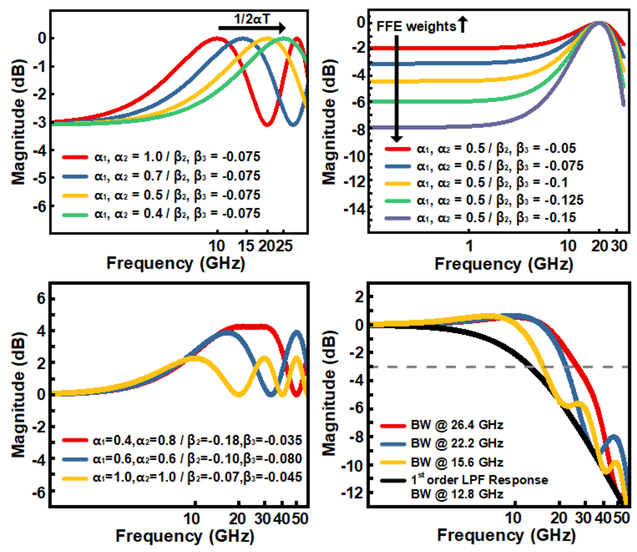


Fig 2. Reconfigurable and Fractionally Spaced FFE

- The reconfigurable tap configuration provides flexibility to adjust which cursor is active, allowing the equalizer to address bias-dependent modulation response issues.
- The 3-tap fractionally spaced feed-forward equalizer effectively compensates for the insufficient bandwidth of a VCSEL device with 14.7-GHz modulation bandwidth.

Optical Receiver

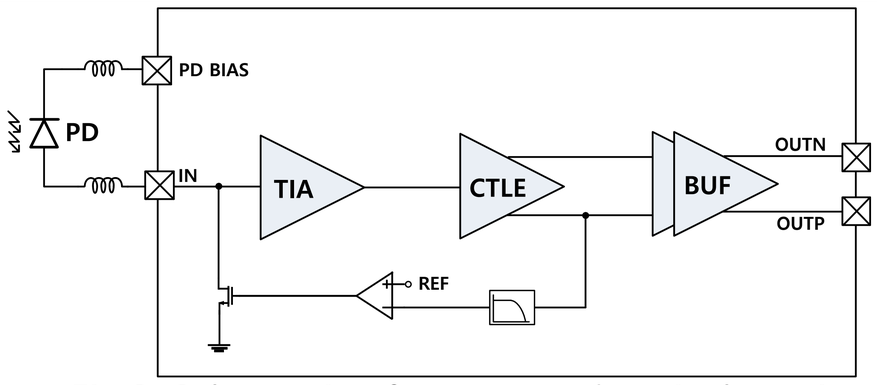


Fig 3. Schematic of a proposed optical receiver.

- The proposed optical receiver consists of a layout-optimized trans-impedance amplifier using a Berkeley analog generator, a continuous-time linear equalizer, a DC offset cancellation loop, an output buffer, and a photodiode.

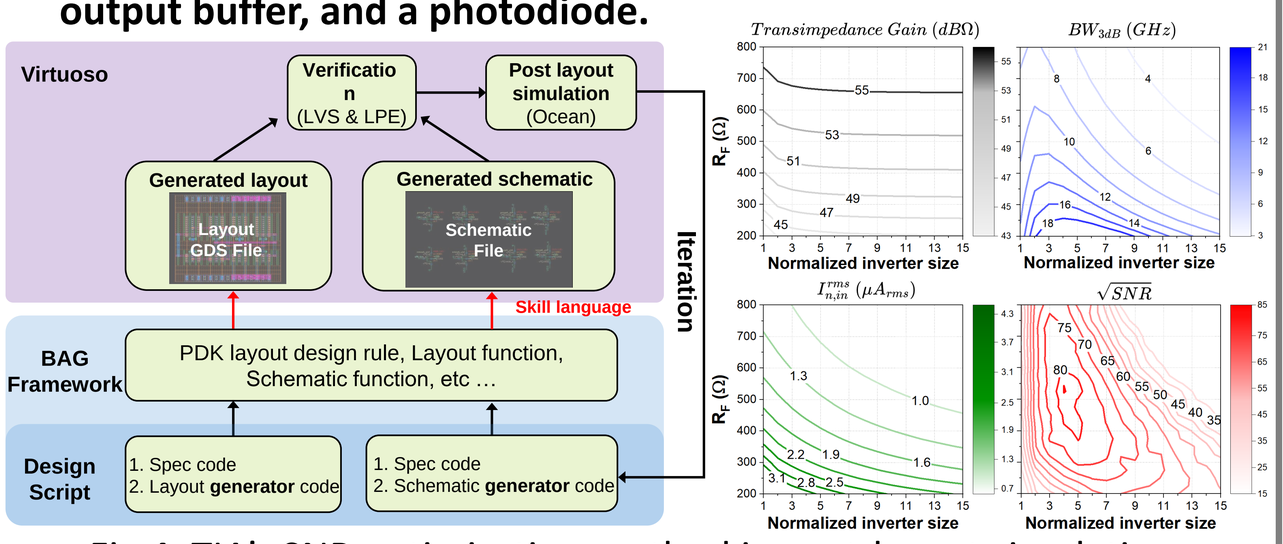


Fig 4. TIA's SNR optimization method in post-layout simulation.

- The inverter sizes and resistance values within the TIA core are parameterized in a parametric sweep process in the layout using the Berkeley analog generator.

Measurement Results

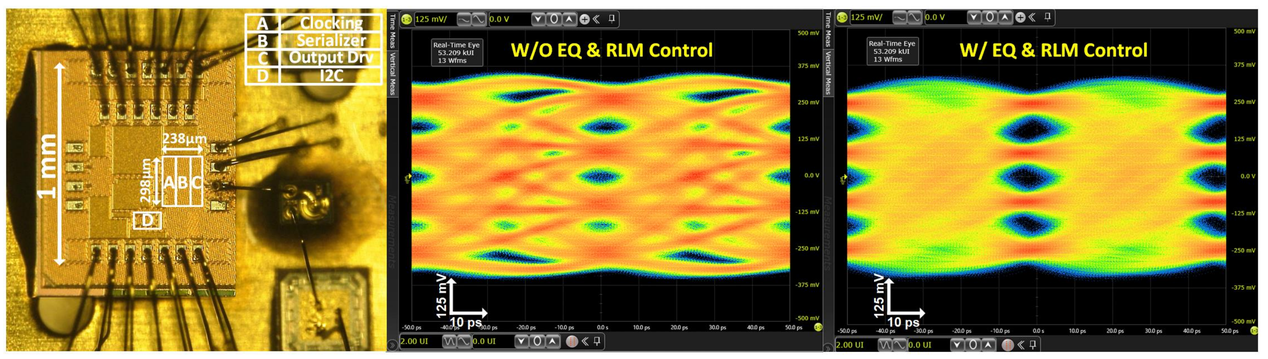


Fig 5. VCSEL driver chip photo with optical eye diagrams at 40-Gb/s.

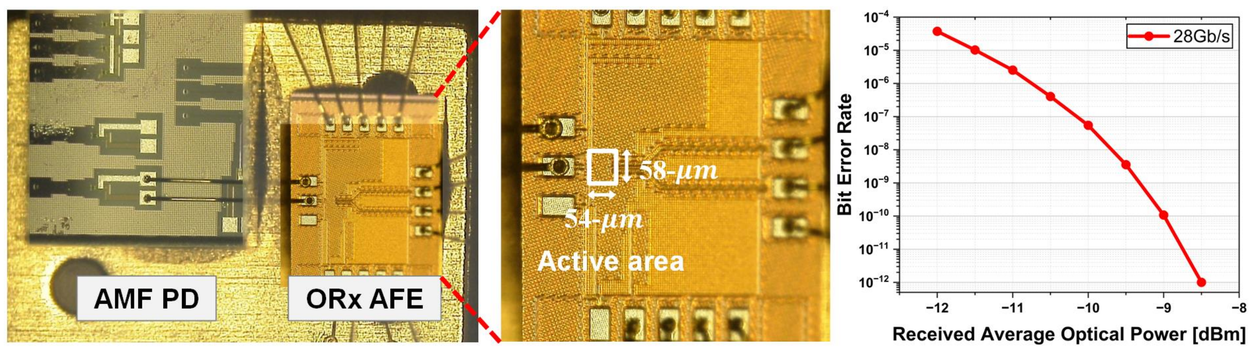


Fig 6. Optical receiver chip photo with measured BER curve at 28-Gb/s.

Comparison table of VCSEL driver

	JSSC '21	JSSC '18	CICC '17	JSSC '24	This Work
Technology	28nm CMOS	14nm CMOS	28nm CMOS	12nm CMOS	28nm CMOS
Data Rate [Gb/s]	56	45	40	50	40
Signaling	NRZ	NRZ	NRZ	PAM-4	PAM-4
Data Sequence	PRBS-10	PRBS-7	PRBS-7	PRBS-9	PRBS-31
Equalization Technique	3-tap FFE, Shunt peaking	Fractional space 2-tap FFE	Complex zero	3-tap FFE	Fractional space 3-tap FFE
VCSEL BW [GHz]	28	18	19	23	14.7
O/E converter BW [GHz]	30	22	35	34	21.5
Core Area [mm^2]	0.024	0.088	0.033	0.086	0.071*
Energy Efficiency [pJ/bit]	1.28*	2.11	0.5	0.97	0.75 / 3.7*
Bandwidth Efficiency [bit/Hz]	2.7	3.2	2.4	2.6	3.3

*Including Serializer & Clocking Circuits

Comparison table of optical receiver

	SOCC '15	RFICS '18	JSSC '18	JSSC '17	This Work
Technology	28nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS	28nm CMOS
Data Rate [Gb/s]	17	25	25	25	28
Signaling	NRZ	NRZ	NRZ	NRZ	NRZ
Data Sequence	PRBS-31	-	PRBS-7	PRBS-15	PRBS-31
Optical Sensitivity @10^{-12} [dBm]	-4.3	-6.8	-0.2*	-10.8	-8.5
Power efficiency [pJ/bit]	-	0.17	1.23	1.13	1.24**
Total area [mm^2]	0.0025	0.0018	0.0056	0.007	0.029

* Optical modulation amplitude ** Including output buffer power consumption

Fig 7. Comparison tables of proposed VCSEL driver and optical receiver.

Conclusion

- The VCSEL driver achieves total energy and bandwidth efficiencies of 3.7 pJ/bit and 3.3 bits/Hz at PAM-4 40-G/bps, respectively.
- The optical receiver AFE achieves the optical sensitivity of −8.5 dBm at 28-Gb/s with post layout optimization.

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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